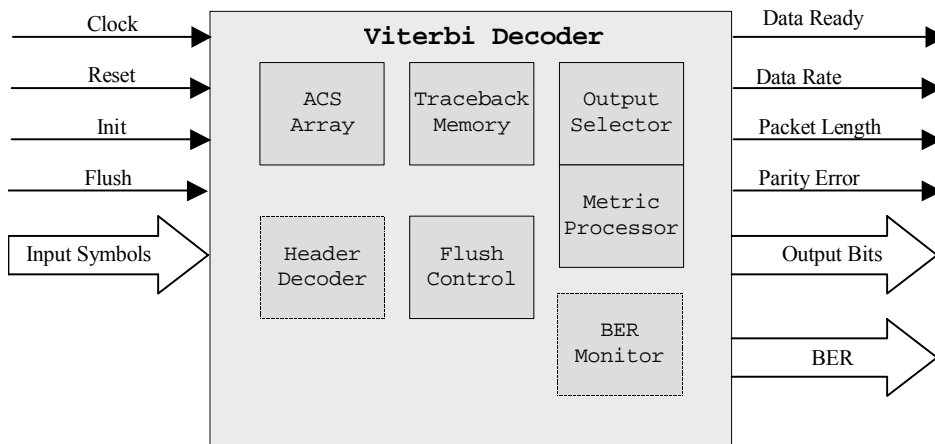


Product Brief

WiMax/WLAN Viterbi Decoder



IP Core Name

R3VIT-WIMAX– Fourth generation
RAM based Viterbi decoder optimized
for WiMax/WLAN (802.16, 802.11a/g)
applications

- b) Capture and decode of packet length, parity & rate
- c) parallel flush capability after trellis closure to reduce latency
- Synchronous single phase design
- Convenient external interface

Features

- Fourth generation soft decision Viterbi decoder targeted for 802.11a/g, 802.16 and other wireless standards.
- Silicon verified in multiple products
- Area/Power efficient RAM based architecture for traceback storage
- Programmable soft decision wordlength
- Automatic internal metric rescaling
- Low latency
- Optimized design allowing high-speed (>54 Mbits/s) operation
- Optional Features:
 - a) BER monitor

Deliverables

- Synthesizable RTL source code in VHDL
- Comprehensive verification test bench and vectors
- C based simulation model & Matlab testbench for system simulation
- Integration documentation

RAD3 IP Cores Series: WiMax/WLAN Viterbi Decoder

Overview

The R3VIT-WIMAX is a second generation Viterbi decoder targeted for WiMax and Wireless LAN applications. The decoder utilizes an advanced area-efficient architecture which places the traceback memory in RAM with no latency penalty.

The design is targeted for use in ASICs and FPGAs.

Input symbol metric pairs are decoded into output data bits by the maximum likelihood Viterbi processor core. Input symbol wordlength is selectable.

Processor core is optimized for decoding the 133,171 encoder used in 802.11a/g and 802.16 applications.

Coding gain is dependent on the chosen traceback depth and soft decision wordlength. Coding gain specifications are available upon request.

Trellis closure to reset decoder state is included. Parallel flush to empty decoder is 8 bits/clock after the trellis is closed.

ASIC implementation (65nm TSMC process)		
Traceback Depth	Soft Decision Wordlength	Typical Clock Speed
40	4	160 MHz
80	8	160 MHz

Traceback Depth	Soft Decision Wordlength	Gates (2-input NAND Equivalent)
40	4	26k gates, 2.5 kbits RAM
80	8	37k gates, 5 kbits RAM

Performance

The Viterbi core easily exceeds the maximum specified throughput of 54 Mbits/s for 802.11a/g.

Maximum clock speed depends on the application process but typically is at least 160 MHz for a 65 nm ASIC process. Clock speeds of greater than 120 MHz have been achieved for FPGA's i.e. Virtex-4. Please contact Rad3 for further details.

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