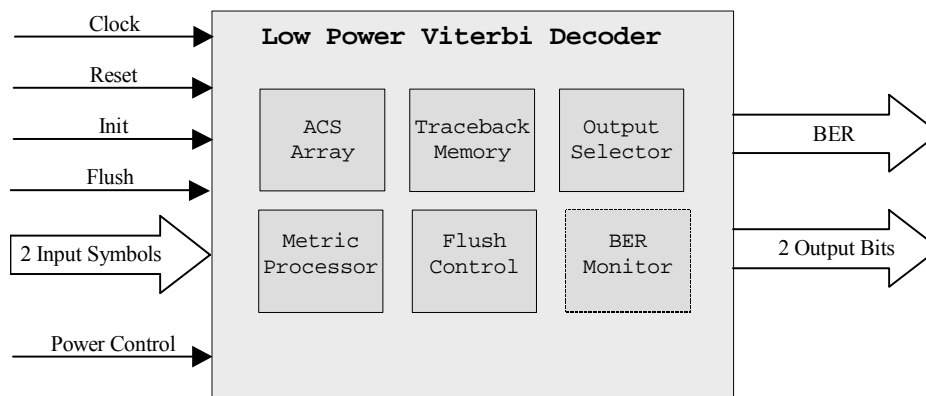


# Product Brief

## WiMedia Ultra Low Power Viterbi Decoder

WiMedia Wireless USB Ultra Low Power Viterbi Decoder



### IP Core Name

#### R3VIT-WUSB-LP

Fourth generation ultra low power RAM based Viterbi decoder optimized for Wireless USB (Multiband OFDM) applications

### Features

- Fourth generation soft decision Viterbi decoder targeted for UWB Multiband OFDM and optimized for low power operation
- Silicon proven
- Ability to dynamically control the power consumption of the decoder
- Area/Power efficient architecture utilizing RAM for survivor path storage
- Parallel input stage allowing two input symbols to be computed in parallel

- Optimized design allowing high-speed (480 Msymbol/s) operation
- Programmable soft decision wordlength
- Automatic internal metric rescaling
- Low latency
- Synchronous single phase design with convenient external interface
- Optional Features:
  - a) BER monitor

### Deliverables

- Synthesizable RTL source code in VHDL or Verilog
- Comprehensive verification test bench and vectors
- Matlab C based simulation model & testbench for system simulation
- Integration documentation

## Overview

The R3VIT-WUSB-LP is a fourth generation Viterbi decoder targeted for WiMedia's Wireless USB Multiband OFDM PHY. The decoder incorporates advanced power saving techniques to allow dynamic reduction of the power consumption with negligible impact on performance. Power consumption can be reduced by up to an order of magnitude relative to standard decoder architectures.

The base decoder architecture utilizes an advanced area-efficient RAM based architecture which places the traceback memory in low-power RAM with no latency penalty.

The decoder supports an input stage with two symbols being processed in parallel enabling extremely high throughput operation. Each input symbol consists of 3 soft values.

The decoder complies with the  $R=1/3, K=7$  code with generator polynomials  $g_0 = [133]_8$ ,  $g_1 = [165]$ ,  $g_2 = [171]_8$  specified in the Multiband OFDM PHY proposal.

Input symbol metric pairs are decoded into output data bits by the maximum likelihood Viterbi processor core. Input symbol wordlength is selectable.

Optional features for this core are as follows:

BER Monitor – re-encode and compare of Viterbi decoder output to input in order to allow BER estimation

The design is targeted for use in ASICs and FPGAs.

## Performance

The Viterbi core achieves  $>480$  MSymbols/s throughput as required for the MB-OFDM specification. The decoder operates at a clock speed of one half the symbol rate. As a result, two output bits are produced per clock cycle.

Coding gain is dependent on the chosen traceback depth and soft decision wordlength. Coding gain specifications are available upon request.

Trellis closure to reset decoder state is included.

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