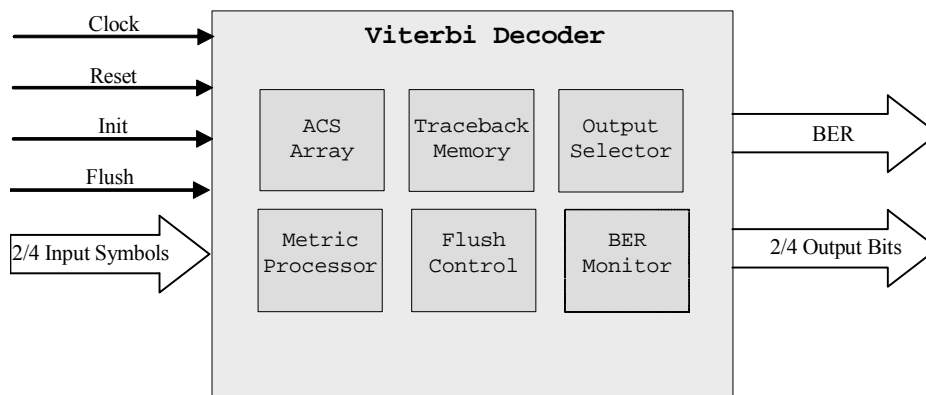


Product Brief

Wireless USB Viterbi Decoder

WiMedia Wireless USB Viterbi Decoder



IP Core Name

R3VIT-WUSB-Third generation RAM based Viterbi decoder optimized for WUSB applications

Features

- Third generation soft decision Viterbi decoder targeted for 802.15.3a
- Silicon proven
- Area/Power efficient architecture utilizing RAM for traceback storage
- Parallel input stage allowing two or four input symbols to be computed in parallel
- Optimized design allowing high-speed (480 Msymbol/s) operation
- Programmable soft decision wordlength
- Automatic internal metric rescaling
- Low latency

- Synchronous single phase design with convenient external interface
- Optional Features:
 - a) Deinterleaver/Depuncturer
 - b) Header decode
 - c) BER monitor
 - d) Parallel flush capability after trellis closure to reduce latency

Deliverables

- Synthesizable RTL source code in VHDL or Verilog
- Comprehensive verification test bench and vectors
- Matlab C based simulation model & testbench for system simulation
- Integration documentation

Overview

The R3VIT-WUSB is a third generation Viterbi decoder targeted for the Multiband OFDM PHY proposed for the Wireless USB. The decoder utilizes an advanced area-efficient RAM based architecture which places the traceback memory in low-power RAM with no latency penalty.

The decoder supports an input stage with either two or four input symbols being processed in parallel enabling extremely high throughput operation. Each input symbol consists of 3 soft values.

The decoder complies with the $R=1/3, K=7$ code with generator polynomials $g_0 = [133]_8$, $g_1 = [165]$, $g_2 = [171]_8$ specified in the Multiband OFDM PHY proposal.

Input symbol metric pairs are decoded into output data bits by the maximum likelihood Viterbi processor core. Input symbol wordlength is selectable.

Optional features for this core are as follows:

Deinterleaver/Depuncturer – accepts FFT output data at a rate of 640 Msoftvalues/s and produces deinterleaved and depunctured input symbols for the Viterbi decoder

BER Monitor – re-encode and compare of Viterbi decoder output to input in order to allow BER estimation

Parallel Flush – Capability to flush Viterbi decoder traceback memory 8-bits at a time after trellis closure resulting in reduced latency.

The design is targeted for use in ASICs and FPGAs.

Performance

The Viterbi core easily achieves >480 Msymbols/s throughput as required for Wireless USB. The decoder operates at a clock speed of either one half or one quarter the symbol rate depending on the selected input processing stage. As a result, two or four output bits are produced per clock cycle respectively.

Coding gain is dependent on the chosen traceback depth and soft decision wordlength. Coding gain specifications are available upon request.

Trellis closure to reset decoder state is included. Parallel flush to empty decoder is 8 bits/clock after the trellis is closed.

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