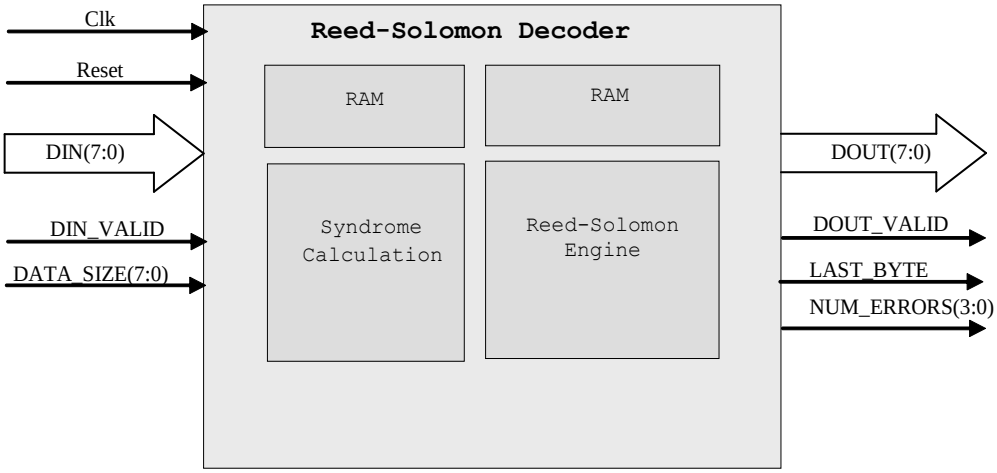
Product Brief

Reed-Solomon Decoder

(255,239) Reed-Solomon Decoder



IP Core Name

R3RSD-255_239
Reed-Solomon Decoder optimized for industry standard RS(255,239) codes

Features

- Optimized for N=255, K=239 & T=8
- Supports variable data block size with fixed length 16 byte parity
- Supports high-speed (>2.6 Gbps) FPGA operation at 333 MHz
- Low latency design 234 clock cycles from last byte in to first byte out
- Able to process a new FEC block every 239 clock cycles
- One byte per clock cycle input
- Outputs number of detected errors
- Synchronous single phase design
- Convenient external interface
- Area efficient design

Deliverables

- Synthesizable RTL source code in VHDL or Verilog
- Comprehensive verification test bench and vectors
- Integration documentation

Overview

The Reed-Solomon decoder is targeted towards a wide range of industry standards which require codeword length N =255 and message length K = 239. The decoder can correct up to T = 8 symbol errors.

The core has extremely low latency and is highly pipelined allowing it to operate at high

RAD3 Communications Inc.
3553 – 31 Street NW, Suite 253
Calgary, AB, Canada
T2L 2K7

web: www.rad3comm.com
email: sales@rad3comm.com

clock speeds i.e >150 MHz.on a Spartan-3 FPGA

The design is targeted for use in ASICs and FPGAs.

Performance

The Reed-Solomon core easily exceeds the 2.66 Gbps operation on FPGA and 3.2 Gbps on ASIC.

Maximum clock speed depends on the application process but typically is at least 400MHz for a 65 nm ASIC process.

ASIC implementation (65 nm TSMC process)		
IP Core Name	**Clock Speed**	**Gates (2-input NAND Eq.)**
R3RSD-255_239	400 MHz	20k gates – includes memory

FPGA Implementation			
Clock Speed	**Device**	**LUTs**	**18k Block RAM's**
333 MHz	XC5VLX30-3	2320	2
150 MHz	XC3SD1800A-5	3150	2

Other Products

RAD3 has a library of IP targeted towards LTE, WiMax 802.16 and other standards. This includes OFDM Modems, Viterbi and LDPC decoders, N-point FFT's, FIR filters and AES encryption cores. Please see RAD3's product section for further details.

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