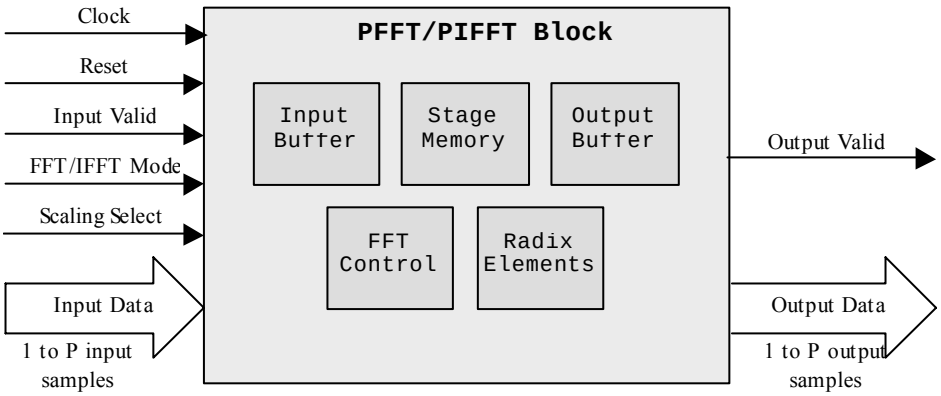
Product Brief

Parallel N-Point FFT/IFFT Core

Parallel N-Point Fast Fourier Transform



IP Core Names

R3PFFT – Parallel N-point FFT/IFFT

Features

- Extremely high throughput through programmable parallelization of input data samples. The core allows 1,2, 4, .., P (P<=N) samples to be computed in parallel for increased data throughput
- Ultra high speed (>3.2 Gsps) continuous time operation
- Configurable number of points, N
- Programmable input and output wordlengths and internal precision
- Area efficient design

Deliverables

- Synthesizable RTL source code in VHDL or Verilog
- Comprehensive verification test bench and vectors in VHDL or Verilog
- Matlab C based bit-correct simulation model and SNR calculator
- Integration documentation and user guide

Overview

The Parallel FFT/IFFT core is targeted for applications in broadband networking, high-speed wireless and image/data processing where extremely high data throughput is required.

The FFT or inverse FFT is performed on the N complex valued input samples. The value of N can be any power of two. In addition, 1 to P (P<=N) samples can be processed in parallel. If 1 sample per cycle operation is chosen the core is equivalent to the SCFFT. The input, output, and internal wordlengths are selectable.

Processor core is optimized for minimum area and maximum throughput. The design is targeted for use in ASICs and FPGAs.

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Performance

The PFFT/IFFT core is able to perform an N-point FFT/IFFT in N/P clock cycles where P represents the number of samples computed in parallel. The throughput is P complex samples per clock cycle. The PFFT/IFFT core processes data continuously with no pauses.

Maximum clock speed depends on the application process and pipelining choices (and hence the final design real estate) but up to 300 MHz for a 0.13 micron ASIC process have been achieved. In order to achieve higher clock rates the latency of the system may increase as pipelining stages are added in the arithmetic.

Signal scaling is controllable by the Scaling Select input signal and for a 64-point FFT could be chosen to yield any power of 2 scaling between 1 and 64 (i.e. 1, 2, 4, 8, …, 64).

The SNR of the block is dependent on the chosen internal wordlength and output wordlength.

The equivalent gate count for the logic area (including RAM requirements) of several PFFTs is shown in Table 1. These FFTs range from 64-point to 4096-point FFTs for 16-bit data paths and values of P (data points computed in parallel) ranging from 1 to 16. Note, that a target clock speed of 100 MHz was chosen for the benchmarks although speeds >300 MHz are easily achievable.

It is worthwhile to note that the gate count scales in less than linear fashion as the number of parallel samples increases. For example a 64-point FFT in which 16 samples are computed in parallel requires only 7.3 times as much area as a 64-point single data sample per cycle FFT core.

Table 1: Gate Count for various N-point 16-bit Parallel FFT's in 0.13µ TSMC Process

Points-N	Parallel Samples - P	Throughput (usec)[1]	Gate Count
64	1	0.512	35,365
	2	0.256	57,377
	4	0.128	97,718
	8	0.064	161,609
	16	0.032	260,070
128	1	1.024	51,192
	2	0.512	80,627
256	1	2.048	63,429
	2	1.024	103,641
512	1	4.096	85,578
	2	2.048	130,068
1024	1	8.192	134,245
	2	4.096	180,903
	4	2.048	281,094
4096	1	16.384	324,984
	2	8.192	405,666
	4	4.096	544,860

Note 1. Clock Rate = 200MHz

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The PFFT has also been synthesized for the Virtex-5 series of FPGAs. Table 2 shows the slice count, Block RAMs, and multiplier blocks used for the FPGA implementation operating at a nominal 100 MHz with 16-bit datapath. Note that speeds above 300 MHz are easily attainable on Virtex-5 devices.

Note that it is possible to decrease the FPGA hardware requirements for the PFFT implementations shown above if a lower clock rate is desired. The multiplier blocks can be replaced with slice based multipliers and the Block RAMs can be replaced with CLB RAMs at the expense of a potentially lower clock rate.

Table 2: Hardware Requirements for N-point 16-bit Parallel FFT's in a Xilinx Virtex-5 FPGA

Points-N	Parallel Samples - P	Throughput (usec)[1]	Slices	RAM's	Mult's
64	1	0.64	690	1	4
	2	0.32	1509	0	8
	4	0.16	2017	0	16
	8	0.08	3323	0[2]	28
1024	1	10.24	1542	7	12
	2	5.12	2145	10	20
	4	2.56	4032	12	40

Note 1. Clock Rate = 100MHz
Note 2. RAM's replaced by Flip-Flop's

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