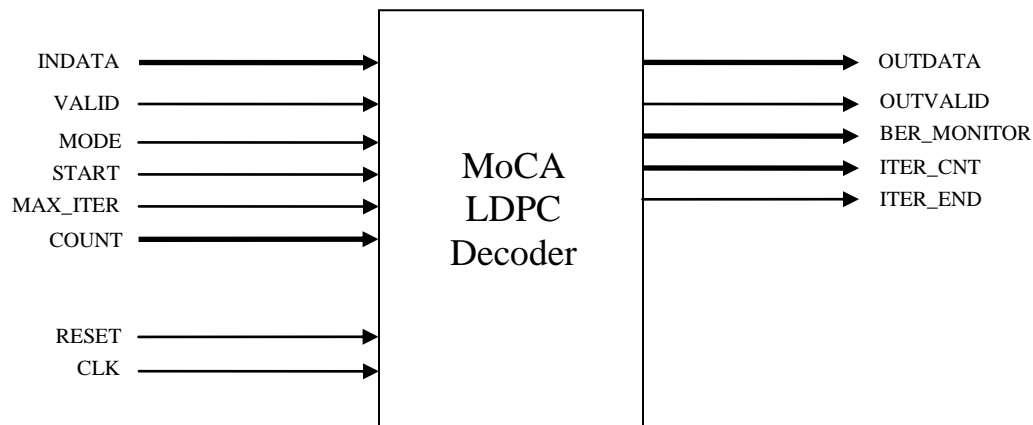


Product Brief

MoCA LDPC Decoder



IP Core Name

R3LDPC-MOCA Decoder for the Multimedia over Coax Alliance (MoCA™) standard.

Features

- Soft decision LDPC decoder targeted for the MoCA 2.0 standard.
- Achieves a throughput of up to 1 Gbit/s depending upon the mode of operation.
- Support for Data (R=0.85) and Signaling (R=0.75) Codewords.
- Provides decoder metrics to allow dynamic tuning for optimum power control.
- Optional LLR Demapper available supporting all 10 required modulations from BPSK to 1024-QAM

Deliverables

- Synthesizable RTL source code in VHDL or Verilog.
- C/C++ system model.
- Comprehensive verification test bench and vectors.

Overview

The R3LDPC-MOCA is an IP Core implemented in RTL that provides a 100% compliant LDPC decoder for the MoCA 2.0 standard. It achieves excellent decoder performance for reasonable decoder complexity.

The MoCA standard specifies a systematic quasi-cyclic LDPC block code (QC-LDPC-BC) of length 4600 bits for data code words and 576-bits signaling code words. LDPC data rates of 0.85 for data and 0.75 for signaling are supported. The decoder supports both rates as two modes of operation.

RAD3 IP Cores Series: MoCA LDPC Decoder

The R3LDPC-MOCA core allows the user to optimize for both power and area by providing a range of decoder parameters. These parameters can either be modified during the design process or even dynamically during normal operation of the decoder.

The design is targeted for use in ASICs and FPGAs.

Performance

The LDPC decoder core provides throughput of up to 1 Gbit/s for both supported code rates with a 150 - 200 MHz clock. Full speed operation can be supported on both ASIC and FPGA platforms.

The R3LDPC-MOCA decoder has excellent BER performance and easily meets the MoCA 2.0 requirements.

Detailed performance curves and data on ASIC/FPGA resource utilization can be provided under NDA.

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