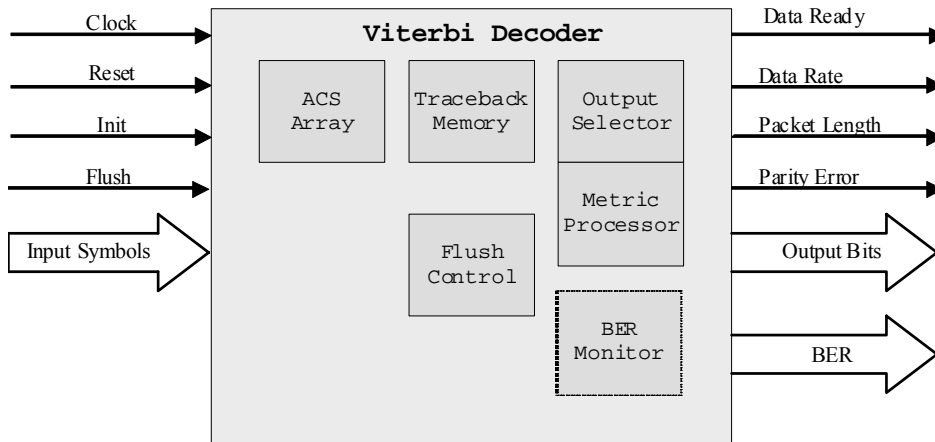


Product Brief

3GPP LTE Viterbi Decoder



IP Core Name

R3VIT-LTE – Fourth generation RAM based Viterbi decoder optimized for LTE (3GPP) applications

- Synchronous single phase design
- Convenient external interface

Features

- Fourth generation soft decision Viterbi decoder targeted for 3GPP LTE
- Area/Power efficient RAM based architecture for traceback storage
- Support for tail biting
- Programmable soft decision wordlength
- Automatic internal metric rescaling
- Low latency for control path processing
- Optimized design allowing high-speed operation
- Optional Features:
 - a) BER monitor

Deliverables

- Synthesizable RTL source code in VHDL
- Comprehensive verification test bench and vectors
- C based simulation model & Matlab testbench for system simulation
- Integration documentation

RAD3 IP Cores Series: LTE Viterbi Decoder

Overview

The R3WIMAX-VIT is fourth generation Viterbi decoder targeted for LTE applications. The decoder utilizes an advanced area-efficient architecture which places the traceback memory in RAM with no latency penalty.

The design is targeted for use in ASICs and FPGAs.

Input symbol metric pairs are decoded into output data bits by the maximum likelihood Viterbi processor core. Input symbol wordlength is selectable.

Processor core is optimized for decoding the 133,165,171 encoder used in 3GPP LTE applications.

the tail biting nature of the LTE convolutional coding and the short packet size.

Coding gain is dependent on the chosen traceback depth and soft decision wordlength. Coding gain specifications are available upon request.

Performance

Maximum clock speed depends on the application process but typically is at least 200 MHz for a 90 nm ASIC process. Clock speeds of greater than 160 MHz have been achieved for FPGA's i.e.Virtex-4. Please contact Rad3 for further details.

The Viterbi core's throughput is approximately equal to 1/3 to 1/2 the target clock frequency i.e 50-80 Mbits/s at 160 MHz clock rate, due to

Typical ASIC implementation (90nm TSMC process)		
Traceback Depth	Soft Decision Wordlength	Typical Clock Speed
40	4	160 MHz
80	8	160 MHz

Traceback Depth	Soft Decision Wordlength	Gates (2-input NAND Equivalent)
40	4	26k gates, 2.5 kbits RAM
80	8	37k gates, 5 kbits RAM

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