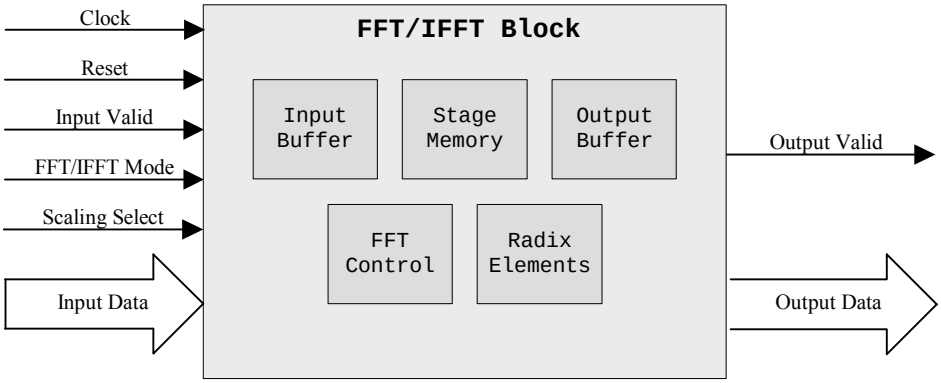
Product Brief

N-Point FFT/IFFT Core

N-Point Fast Fourier Transform



IP Core Names

R3FFT – N-point FFT/IFFT

Features

- High speed (>200 Msps) continuous time operation
- Configurable length FFT/IFFT block
- Programmable input and output word lengths and internal precision
- Area efficient design
- Silicon verified in multiple products
- Optimized for WLAN (802.11, 802.16), DVB and other OFDM standards

Deliverables

- Synthesizable RTL source code in VHDL or Verilog
- Comprehensive verification test bench and vectors in VHDL or Verilog
- Matlab C based bit-correct simulation model and SNR calculator
- Integration documentation and user guide

Overview

The FFT or inverse FFT is performed on the N complex valued input samples. The value of N can be any power of two. The input, output, and internal wordlengths are selectable.

Processor core is optimized for minimum area and maximum throughput.

The design is targeted for use in ASICs and FPGAs.

Performance

The FFT/IFFT core is able to perform an N-point FFT/IFFT in N clock cycles. The throughput is one complex sample per clock cycle. The latency depends on the desired clock frequency and ASIC process or FPGA target device. The FFT/IFFT core processes data continuously with no pauses.

Maximum clock speed depends on the application process and pipelining choices (and hence the final design real estate) but

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frequencies of 300 MHz and above for a 0.13 micron ASIC process have been achieved. In order to achieve higher clock rates the latency of the system may increase as pipelining stages are added in the arithmetic.

Signal scaling is controllable by the Scaling Select input signal and for a N-point FFT could be chosen to yield any power of 2 scaling between 1 and N (i.e. 1, 2, 4, 8, …, N). The SNR of the block is dependent on the chosen internal wordlength and output wordlength.

The equivalent gate count for the logic area (including RAM requirements) of several FFTs running at a nominal 100 MHz clock rate is shown in Table 1. These FFTs range from 64-point to 4096-point FFTs with 16-bit data paths.

Table 1: Gate Count for various N-point 16-bit FFT's in 0.13µ TSMC Process

Points-N	Throughput (usec)[1]	Gate Count
64	0.512	35,365
128	1.024	51,192
256	2.048	63,429
512	4.096	85,578
1024	8.192	134,245
4096	16.384	324,984

The FFT has also been synthesized for the Xilinx Virtex-5 series of FPGAs. Table 2 shows the slice count, Block RAMs, and multiplier blocks used for the FPGA implementation operating at 100 MHz with 16-bit datapath. Higher clock rates above 300 MHz are easily achievable if required.

Table 2: Xilinx Virtex-5 Hardware Requirements for Various 16-bit FFTs

Points	Slices	BRAM	DSP48's
64	690	1	4
128	831	2	8
256	925	3	8
512	1046	5	8
1024	1174	7	12

Note that it is possible to decrease the FPGA hardware requirements for the FFT implementations if a lower clock rate is desired. The multiplier blocks can be replaced with slice based multipliers and the Block RAMs can be replaced with CLB RAMs at the expense of a potentially lower clock rate.

Note 1: Clock Rate = 100 MHz

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