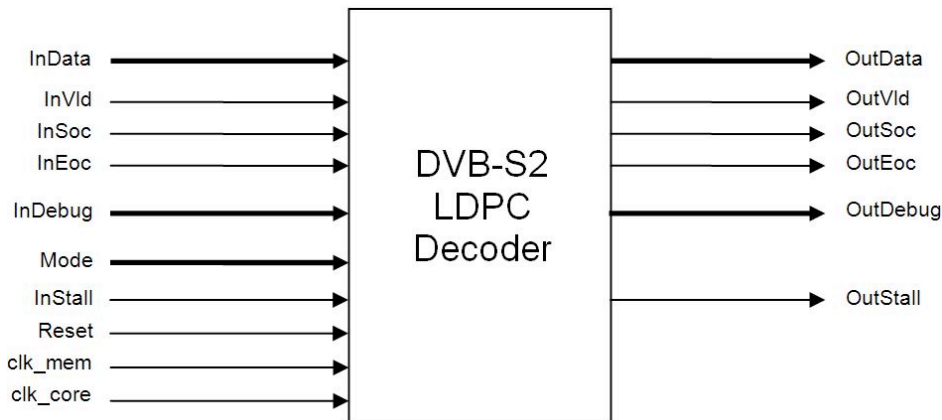


Product Brief

DVB-S2 LDPC Decoder



IP Core Name

R3LDPC-DVB-S2 Decoder for digital video broadcast – satellite – second generation (DVB-S2) standard.

Features

- Soft decision Belief Propagation (BP) LDPC decoder targeted for the DVB-S2 standard.
- Meets the throughput requirements of the DVB-S2 standard.
- Provides decoder metrics to allow dynamic tuning for optimum power control.
- Implements upstream/downstream flow control and data buffering for easy integration.
- Verified on FPGA platform.

Deliverables

- Synthesizable RTL source code in VHDL.
- Comprehensive verification test bench and vectors.
- LDPC Visualizer development environment.
- Opal Kelly XEM3010 FPGA platform (Optional extra).

Overview

The R3LDPC-DVB-S2 is an IP Core implemented in RTL that provides a 100% compliant LDPC decoder for the DVB-S2 standard. It achieves excellent decoder performance for reasonable decoder complexity by using a propriety version of the belief propagation algorithm.

The DVB-S2 standard specifies LDPC codes of lengths 16200 bits for short frames and 64800 bits for long frames. Various code rates are supported and may be dynamically changed from one frame to the next; they include 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, and 9/10. The decoder supports all rates as modes of operation.

The R3LDPC-DVB-S2 core allows the user to optimize both power and area by providing a range of decoder parameters. These parameters can either be modified during the design process or even dynamically during normal operation of the decoder.

The design is targeted for use in ASICs and FPGAs.

Performance

The LDPC decoder meets the throughput requirements of the standard.

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LDPC Visualizer – FPGA Platform

The LDPC Visualizer is an FPGA based prototyping kit that implements the R3LDPC-DVB-S2 in a Xilinx Spartan-3 along with noise generators, traffic generators, and a bit error rate counter. The platform also includes a GUI type interface to allow the user to experiment with the parameters of the R3LDPC-DVB-S2.

The platform is useful for exploring the configuration of the R3LDPC-DVB-S2 and for obtaining low BER results in short periods of time. The entire platform has been optimized to run on an Opal Kelly XEM3010 board (www.opalkelly.com).