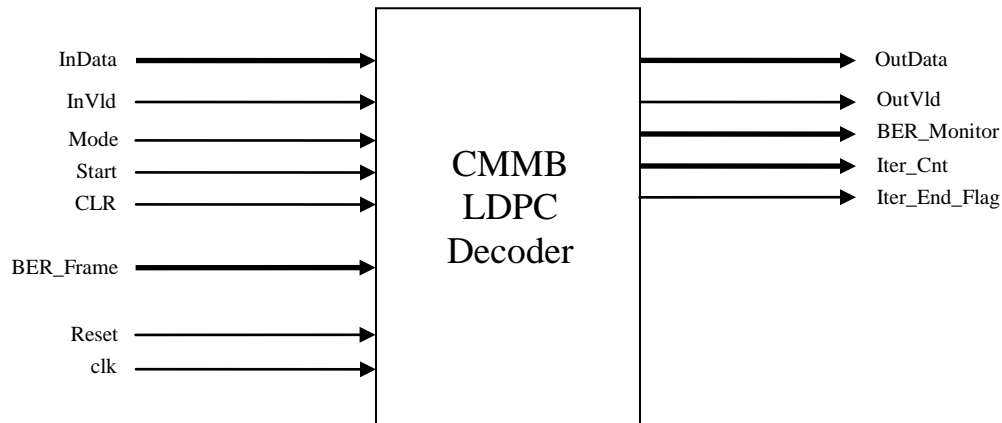


# Product Brief

## CMMB (STiMi) LDPC Decoder



### IP Core Name

R3LDPC-CMMB Decoder for the GY/T220.1-2006 Mobile-TV standard. Based on the satellite and terrestrial interactive multiservice infrastructure (STiMi) air interface, which is part of the China Multimedia Mobile Broadcasting (CMMB) family of standards.

### Features

- Soft decision Belief Propagation (BP) LDPC decoder targeted for GY/T220.1-2006 (STiMi) standard.
- Achieves a throughput of up to 17 Mbps depending upon mode of operation.
- Provides decoder metrics to allow dynamic tuning for optimum power control.
- Silicon proven

- Provides the ability to count and report Bit Error Rate (BER) over a user-specified number of decoded frames.

### Deliverables

- Synthesizable RTL source code in VHDL or Verilog.
- C/C++ system model.
- Comprehensive verification test bench and vectors.

### Overview

The R3LDPC-CMMB is an IP Core implemented in RTL that provides a 100% compliant LDPC decoder for the GY/T220.1-2006 (STiMi) DVB standard. It achieves excellent decoder performance for reasonable decoder complexity by using a propriety version of the belief propagation algorithm.

## RAD3 IP Cores Series: CMMB (STiMi) LDPC Decoder

The STiMi standard specifies quasi-cyclic LDPC codes of length 9216 bits and code rates  $\frac{1}{2}$  and  $\frac{3}{4}$ . The decoder supports both rates as two modes of operation.

The R3LDPC-CMMB core allows the user to optimize both power and area by providing a range of decoder parameters. These parameters can either be modified during the design process or even dynamically during normal operation of the decoder.

The design is targeted for use in ASICs and FPGAs.

### Performance

The LDPC decoder core provides throughput of 11.2 Mbps for code rate  $\frac{1}{2}$  and 16.9 Mbps for code rate  $\frac{3}{4}$  with a 60 MHz clock, which meets the throughput requirements of the standard.

It delivers a Bit Error Rate (BER) of  $10^{-4}$  at an input SNR (Eb/No) of 1.6 dB (2.65 dB) for the Rate 1/2 (3/4) code under Gaussian noise conditions.

The design uses approximately 100,000 gates and 42KB of memory, which includes the LDPC decoder as well as the col\_order step specified by the standard. 40 to 100 MHz clock speed range may be used.

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